C2DTUACOMR03 – CFP2 ACO Dual Fibre DWDM

DWDM Tunable 6.25GHz / Analog Coherent / 100G & 200G

For your product safety, please read the following information carefully before any manipulation of the transceiver:

ESD
This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.

LASER SAFETY
This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

1. Overview

C2DTUACOMR03 is a high performance CFP2 ACO transceiver module for 100Gbps DP-QPSK or 200Gbps DP-16QAM data links over two single mode fibres. The amplified narrow linewidth tunable laser is shared between the transmitter and receiver sections. A tapped monitor diode is used to control the optical output power.

The receiver module is performing the coherent intradyne reception and O/E conversion of the incoming optical signal after being mixed with a local optical oscillator. Four pairs of balanced photo detectors perform quadratic detection and produce the I and Q components of the two orthogonal polarizations (X and Y).

This transceiver module is compliant with the CFP Multisource Agreement (MSA) and hot pluggable. Always contact Skylane Optics® commercial agents for compatibility with different equipment platforms.

2. Features

- Hot Pluggable CFP2 Multi-Source Agreement compliant Hardware
- OIF-CFP2-ACO-01.0, Implementation Agreement for CFP2
- Class 2 implementation with Linear Driver and TIA
- Tunable C-band Transmitter
- Transmitter Variable Optical Attenuator (VOA)
- Coherent Receiver
- Operating temperature range 0°C to 70°C
- CFP2 Power Class 4 (< 12W)
- Single +3.3V Power Supply
- CFP MSA Management Interface (MDIO)

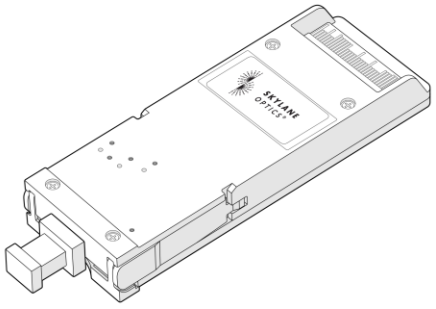


Figure 1. CFP2 Dual Fibre
(non-binding illustration)

3. Applications

- 100G DP-QPSK
- 200G DP-16QAM

4. Optical Interface

P/N	Wavelength	Protocol	Optical Output Power[1] [dBm]	Optical Receiver Sensitivity[2] [dBm]	Optical Receiver Overload[3] [dBm]
C2DTUACOMR03	ITU DWDM	100G 200G	-15 to 1	≤ -25	0

1. EOL over operating temperature range, settable in steps of 0.1dB
2. See section 5.4 for definitions
3. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers (optical loop back) before ensuring that proper optical attenuation is used

5. Technical Parameters

5.1. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit	Notes
Storage temperature	-40		85	°C	
Operating Case Temperature	0		70	°C	
Relative Humidity			85	%	Non-Condensing
Power Supply Voltage	3.2	3.3	3.4	V	
Power Supply Current			3.75	A	
Power Dissipation			12	W	

5.2. General Specifications

Parameter	Min	Typ	Max	Unit	Notes
Symbol Rate			34.17	GBd	4

4. Corresponding to the maximum bit rates 136.68Gbps (DP-QPSK) and 273.36Gbps (DP-16QAM)

5.3. Transmitter Optical Specifications

Parameter	Min	Typ	Max	Unit	Notes
Average Output Power	-15		1	dBm	5, 6
Output Power Accuracy	-1		1	dB	6, 7
Centre Wavelength Range	1528.77		1568.36	nm	
Frequency Grid Setting	6.25			GHz	8
Centre Wavelength	λ_T -13	λ_T	λ_T +13	pm	8

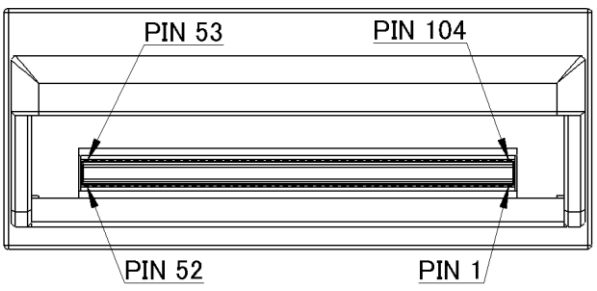
5. The output power is settable in steps of 0.1 dB within the specified wavelength range
6. Output power coupled into a 9/125 µm single mode fibre
7. Difference between the set value and actual value
8. Per ITU-T G.694.1 flexible DWDM grid definition

5.4. Receiver Optical Specifications

Parameter	Min	Typ	Max	Unit	Notes
Receiver Operating Wavelength	1528.77		1567.54	nm	
Receiver Input Power Range	-18		0	dBm	9
	-13		0		10
	-25		0		11
OSNR Tolerance		11.5		dB	12
		19			13

9. An input power in this range guarantees optimum OSNR performance, QPSK
10. An input power in this range guarantees optimum OSNR performance, 16QAM
11. OSNR > 30dB, QPSK
12. BER = 3×10^{-2}, QPSK, 34.2GBd symbol rate, -18 to odBm input power
13. BER = 3×10^{-2}, 16QAM, 34.2GBd symbol rate, -13 to odBm input power

6. Transceiver Electrical Pad Layout



TOP

BOTTOM

Figure 2. Transceiver Electrical Pad Layout

7. Module Electrical Pin Definition

Pin	Symbol	I/O	Description	Logic	Pin	Symbol	I/O	Description	Logic
1	GND		Ground		53	GND		Ground	
2	NC		Do not connect		54	NC		Do not connect	
3	NC				55	NC			
4	GND		Ground		56	GND		Ground	
5	NC		Do not connect		57	RX_YQn	O	Rx YQ output RF signal (RF mapping [0,0,0])	
6	NC				58	RX_YQp			
7	3.3V_GND		Ground		59	GND		Ground	
8	3.3V_GND				60	RX_YIn	O	Rx YI output RF signal (RF mapping [0,0,0])	
9	3.3V		3.3V Power Supply		61	RX_YIp			
10	3.3V				62	GND		Ground	
11	3.3V				63	RXMGCYQ	I	Rx YQ/YI gain control (RF mapping [0,0,0])	
12	3.3V				64	RXMGCYI			
13	3.3V_GND		Ground		65	GND		Ground	
14	3.3V_GND				66	RXMGCXQ	I	Rx XQ/YI gain control (RF mapping [0,0,0])	
15	VND_IO_A		Do not connect		67	RXMGCXI			
16	VND_IO_B				68	GND		Ground	
17	PRG_CNTL1	I	Programmable Control 1	LVCMOS w/ PUR	69	RX_XQn	O	Rx XQ output RF signal (RF mapping [0,0,0])	
18	PRG_CNTL2		Programmable Control 2		70	RX_XQp			
19	PRG_CNTL3		Programmable Control 3		71	GND		Ground	
20	PRG_ALRM1	O	Programmable Alarm 1	LVCMOS	72	RX_XIn	O	Rx XI output RF signal (RF mapping [0,0,0])	
21	PRG_ALRM2		Programmable Alarm 2		73	RX_XIp			
22	PRG_ALRM3		Programmable Alarm 3		74	GND		Ground	
23	GND		Ground		75	NC		Do not connect	
24	TX_DIS	I	Transmitter Disable	LVCMOS w/ PUR	76	NC			
25	RX_LOS	O	Loss of Optical Input Signal	LVCMOS	77	GND		Ground	
26	MOD_LOPWR	I	Module Low Power Mode	LVCMOS w/ PUR	78	REFCLKp		Not Used	
27	MOD_ABS	O	Module Absent Indicator	GND	79	REFCLKn			
28	MOD_RSTn	I	Module Reset	LVCMOS w/ PDR	80	GND		Ground	
29	GLB_ALRMn	O	Global Alarm	LVCMOS (open drain)	81	NC		Do not connect	
30	GND		Ground		82	NC			
31	MDC	I	Management Data Clock	1.2V CMOS	83	GND		Ground	
32	MDIO	I/O	Management bi-dir. Data	1.2V CMOS	84	TX_YQn	I	Tx YQ input RF signal (RF mapping [0,0,0])	
33	PRTADR0	I	MDIO Physical Port addr. bit0	1.2V CMOS	85	TX_YQp			
34	PRTADR1		MDIO Physical Port addr. bit1		86	GND		Ground	
35	PRTADR2		MDIO Physical Port addr. bit2		87	TX_YIn	I	Tx YI input RF signal (RF mapping [0,0,0])	
36	VND_IO_C		Do not connect		88	TX_YIp			
37	VND_IO_D				89	GND		Ground	
38	VND_IO_E				90	NC		Do not connect	
39	3.3V_GND		Ground		91	NC			
40	3.3V_GND		Ground		92	GND		Ground	
41	3.3V		3.3V Power Supply		93	NC		Do not connect	
42	3.3V				94	NC			
43	3.3V				95	GND		Ground	
44	3.3V				96	TX_XQn	I	Tx XQ input RF signal (RF mapping [0,0,0])	
45	3.3V_GND		Ground		97	TX_XQp			
46	3.3V_GND				98	GND		Ground	
47	NC		Do not connect		99	TX_XIn	I	Tx XI input RF signal (RF mapping [0,0,0])	
48	NC				100	TX_XIp			
49	GND		Ground		101	GND		Ground	
50	NC		Do not connect		102	NC		Do not connect	
51	NC				103	NC			
52	GND		Ground		104	GND		Ground	

8. Register Allocation

The total CFP register space (from 8000h to FFFFh) is logically divided into 8 pages with each page starting at even hex thousand, that is, 8000h, 9000h, A000h, …, F000h, with each page further divided into 32 tables.
The CFP MSA specifies the starting address of all non-volatile registers (NVR) at 8000h (8 NVR tables in total).
Page A000h is allocated for volatile registers (VR). The CFP MSA specifies four VR tables for module configuration, control, and various DDM related functions.

Start Address (hex)	End Address (hex)	Table Name and Description
0000	7FFF	Reserved for IEEE 802.3 use
8000	807F	CFP NVR 1. Basic ID registers
8080	80FF	CFP NVR 2. Extended ID registers
8100	817F	CFP NVR 3. Network lane specific registers
8180	81FF	CFP NVR 4
8200	83FF	MSA Reserved
8400	847F	Vendor NVR 1. Vendor data registers
8480	84FF	Vendor NVR 2. Vendor data registers
8500	87FF	Reserved by CFP MSA
8800	887F	User NVR 1. User data registers
8880	88FF	User NVR 2. User data registers
8900	8EFF	Reserved by CFP MSA
8F00	8FFF	Reserved for User private use
9000	9FFF	Reserved for vendor private use
A000	A07F	CFP Module VR 1. CFP Module level control and DDM registers
A080	A0FF	MLG VR 1. MLG Management Interface registers
A100	A1FF	Reserved by CFP MSA
A200	A27F	Network Lane VR 1. Network lane specific registers
A280	A2FF	Network Lane VR 2. Network lane specific registers
A300	A37F	Network Lane VR 3. Network Lane n Vendor Specific FAWS Registers
A380	A3FF	Reserved by CFP MSA
A400	A47F	Host Lane VR 1. Host lane specific registers
A480	ABFF	Reserved by CFP MSA
AC00	AFFF	Common Data Block Registers
B000	BFFF	Allocated for OIF MSA-100GLH modules
C000	FFFF	Reserved by CFP MSA

Figure 3. Register of a CFPx

9. Ordering Information

Part Number	Description
C2DTUACOMR03	CFP2 ACO, DWDM, Tx (tunable), Rx (coherent), 100G DP-QPSK / 200G DP-16QAM, dual LC connector, 0°C to 70°C, DDM

10. Document Revision Information

Revision	Description
A	Initial release

Skylane Optics® supplies a broad range of optical transceivers. Our engineers work closely with our customers to find the best solutions for every application. We are committed to provide high quality products and services to our customers.

For questions on this product please contact:
support@skylaneoptics.com