CF2QD040C10D –CFP2 Dual Fibre

1310nm* / 40km / 100GBASE – ER4 & OTN OTU4

*1310nm LAN-WDM 800GHz

For your product safety, please read the following information carefully before any manipulation of the transceiver:

ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.

LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

1. Overview

CF2QD040C10D is a high performance CFP2 transceiver module for 100 Gigabit Ethernet and OTN OTU4 data links over a single mode fibre pair. The maximum reach is 40km. The four transmitters are cooled 1310nm LAN-WDM Electro-Absorption Modulated Lasers (EML) generating four optical 25Gbps output signals, which are multiplexed together at the optical output port. The receiver consists of four PIN photodiodes and a Semiconductor Optical Amplifier (SOA) which detect (after optical de-multiplexing) the four 25Gbps optical input signals.
This transceiver module is compliant with the CFP Multisource Agreement (MSA) and hot pluggable. Always contact Skylane Optics® commercial agents for compatibility with different equipment platforms.

2. Features

- CFP Multi-Source Agreement compliant
- Hot pluggable CFP2 footprint
- Supports 103.125 and 111.810Gbps Data Rates
- CEI-28G-VSR Electrical Interface
- Dual LC Optical Connector
- 4× cooled 1310nm LAN-WDM EML Transmitters
- 4× PIN Receivers + SOA
- Up to 40km Point-to-Point Transmission on Single Mode Fibre
- Operating temperature range 0°C to 70°C
- Power Dissipation < 9W
- Single +3.3V Power Supply
- CFP MSA MDIO Management Interface

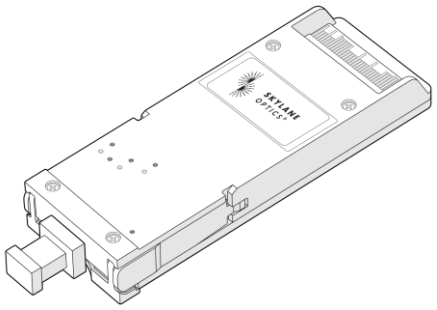

Figure 1. CFP2 Dual Fibre
(non-binding illustration)

3. Applications

- IEEE 802.3ba 100GBASE-ER4
- ITU-T G.959.1 4I1-9C1F

4. Optical Interface

P/N	Wavelength	Protocol	Optical Output Power[1] [dBm]	Stressed Receiver Sensitivity[2] (OMA) [dBm]	Optical Receiver Overload[3] [dBm]	Link Length[1,4] [km]
CF2QD040C10D	1310nm LAN-WDM 800GHZ	100GBASE-ER4	3.1 to 8.9	≤ -17.9	4.5	≤ 40
		Protocol	**Optical Output Power[1] [dBm]**	**Equivalent Receiver Sensitivity[5] [dBm]**	**Optical Receiver Overload[3] [dBm]**	
		G.959.1 4I1-9C1F	3.1 to 8.9	≤ -23.2	4.5	

1. EOL over operating temperature range
2. 25.78Gbps, BER≤ 10^{-12}, PRBS 2^{31}-1, each lane
3. The optical input to each lane of the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used
4. Cabled optical fibre as per IEEE 802.3-2012
5. BER≤10^{-12}, ER≥8dB, with FEC. The BER can be significantly higher at the input to the FEC decoder

5. Technical Parameters

5.1. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit	Notes
Storage temperature	-40		85	°C	
Operating Case Temperature	0		70	°C	
Relative Humidity	5		95	%	Non-Condensing
Power Supply Voltage	3.2	3.3	3.4	V	
Power Supply Current			2900	mA	
Power Dissipation			9	W	

5.2. Transmitter Optical Specifications

100GBASE-ER4					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Data Rate, each Lane		25.78125		Gbps	6
Aggregated Data Rate		103.125		Gbps	6
Average Output Power			8.9	dBm	7
Average Output Power, each Lane	-2.9		2.9	dBm	7,8
Launched OMA, each Lane	0.1		4.5	dBm	7
Difference in launched Power between any two Lanes			3.6	dB	9
Centre Wavelength, Optical Lanes 0 to 3	1294.53	1295.56	1296.59	nm	
	1299.02	1300.05	1301.09		
	1303.54	1304.58	1305.63		
	1308.09	1309.14	1310.19		
Transmitter and Dispersion Penalty (TDP), each Lane			2.5	dB	
Extinction Ratio, each Lane	8			dB	
4I1-9C1F					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Data Rate, each Lane		27.952		Gbps	10
Aggregated Data Rate		111.810		Gbps	10
Average Output Power			8.9	dBm	7
Average Output Power, each Lane	-2.7		2.9	dBm	7
Output Power Difference between any two Lanes			3.6	dB	
Centre Wavelength, Optical Lanes 0 to 3	1294.53	1295.56	1296.59	nm	
	1299.02	1300.05	1301.09		
	1303.54	1304.58	1305.63		
	1308.09	1309.14	1310.19		
Optical Path Penalty			2.5	dB	
Extinction Ratio, each Lane	8			dB	

6. IEEE 802.3-2012
7. Output power coupled into a 9/125 µm single mode fibre
8. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
9. Average and OMA
10. ITU-T G.959.1 (02/12), optical interface 4I1-9C1F

5.3. Receiver Optical Specifications

100GBASE-ER4					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Operating Wavelength, Optical Lanes 0 to 3	1294.53	1295.56	1296.59	nm	
	1299.02	1300.05	1301.09		
	1303.54	1304.58	1305.63		
	1308.09	1309.14	1310.19		
Average Receive Power, each Lane	-20.9		4.5	dBm	11
Receiver Sensitivity (OMA), each Lane			-21.4	dBm	12
Stressed Receiver Sensitivity (OMA), each Lane			-17.9	dBm	13
Difference in receive power between any two lanes (OMA)			4.5	dB	9
4I1-9C1F					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Operating Wavelength, Optical Lanes 0 to 3	1294.53	1295.56	1296.59	nm	
	1299.02	1300.05	1301.09		
	1303.54	1304.58	1305.63		
	1308.09	1309.14	1310.19		
Average Receive Power, each Lane	-20.7		4.5	dBm	14
Equivalent Receiver Sensitivity, each Lane			-23.2	dBm	14
Input Power Difference between any two Lanes			4.5	dB	

11. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
12. Receiver sensitivity (OMA), each lane (max) is informative
13. 25.78Gbps, BER≤10^{-12}, PRBS 2^{31}-1
14. 27.95Gbps, BER≤10^{-12}, ER≥8dB, with FEC. The BER can be significantly higher at the input to the FEC decode

6. Transceiver Electrical Pad Layout

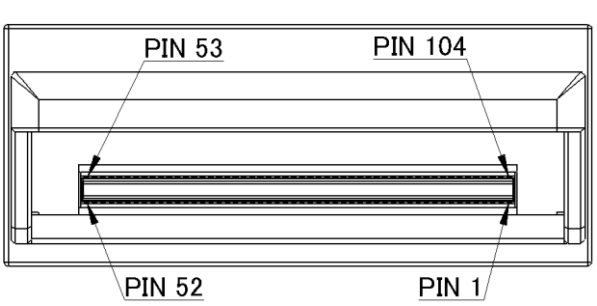

Figure 2. Transceiver Electrical Pad Layout

7. Module Electrical Pin Definition

Pin	Symbol	I/O	Description	Logic	Pin	Symbol	I/O	Description	Logic
1	GND		Ground		53	GND		Ground	
2	TX_MCLKn		Not for normal use		54	NC		Do not connect	
3	TX_MCLKp				55	NC			
4	GND		Ground		56	GND		Ground	
5	NC		Do not connect		57	RX0p	O	Ch0 25Gbps Receive Output	CML
6	NC				58	RX0n			
7	3.3V_GND		Ground		59	GND		Ground	
8	3.3V_GND				60	RX1p	O	Ch1 25Gbps Receive Output	CML
9	3.3V		3.3V Power Supply		61	RX1n			
10	3.3V				62	GND		Ground	
11	3.3V				63	NC		Do not connect	
12	3.3V				64	NC			
13	3.3V_GND		Ground		65	GND		Ground	
14	3.3V_GND				66	NC		Do not connect	
15	VND_IO_A		Do not connect		67	NC			
16	VND_IO_B				68	GND		Ground	
17	PRG_CNTL1	I	Programmable Control 1	LVCMOS w/ PUR	69	RX2p	O	Ch2 25Gbps Receive Output	CML
18	PRG_CNTL2		Programmable Control 2		70	RX2n			
19	PRG_CNTL3		Programmable Control 3		71	GND		Ground	
20	PRG_ALRM1	O	Programmable Alarm 1	LVCMOS	72	RX3p	O	Ch3 25Gbps Receive Output	CML
21	PRG_ALRM2		Programmable Alarm 2		73	RX3n			
22	PRG_ALRM3		Programmable Alarm 3		74	GND		Ground	
23	GND		Ground		75	NC		Do not connect	
24	TX_DIS	I	Transmitter Disable	LVCMOS w/ PUR	76	NC			
25	RX_LOS	O	Loss of Optical Input Signal	LVCMOS	77	GND		Ground	
26	MOD_LOPWR	I	Module Low Power Mode	LVCMOS w/ PUR	78	REFCLKp		Not Used	
27	MOD_ABS	O	Module Absent Indicator	GND	79	REFCLKn			
28	MOD_RSTn	I	Module Reset	LVCMOS w/ PDR	80	GND		Ground	
29	GLB_ALRMn	O	Global Alarm	LVCMOS (open drain)	81	NC		Do not connect	
30	GND		Ground		82	NC			
31	MDC	I	Management Data Clock	1.2V CMOS	83	GND		Ground	
32	MDIO	I/O	Management bi-dir. Data	1.2V CMOS	84	TX0p	I	Ch0 25Gbps Transmit Input	CML
33	PRTADR0	I	MDIO Physical Port addr. bit0	1.2V CMOS	85	TX0n			
34	PRTADR1		MDIO Physical Port addr. bit1		86	GND		Ground	
35	PRTADR2		MDIO Physical Port addr. bit2		87	TX1p	I	Ch1 25Gbps Transmit Input	CML
36	VND_IO_C		Do not connect		88	TX1n			
37	VND_IO_D				89	GND		Ground	
38	VND_IO_E				90	NC		Do not connect	
39	3.3V_GND		Ground		91	NC			
40	3.3V_GND		Ground		92	GND		Ground	
41	3.3V		3.3V Power Supply		93	NC		Do not connect	
42	3.3V				94	NC			
43	3.3V				95	GND		Ground	
44	3.3V				96	TX2p	I	Ch2 25Gbps Transmit Input	CML
45	3.3V_GND		Ground		97	TX2n			
46	3.3V_GND				98	GND		Ground	
47	NC		Do not connect		99	TX3p	I	Ch3 25Gbps Transmit Input	CML
48	NC				100	TX3n			
49	GND		Ground		101	GND		Ground	
50	RX_MCLKn		Not for normal use		102	NC		Do not connect	
51	RX_MCLKp				103	NC			
52	GND		Ground		104	GND		Ground	

8. Register Allocation

The total CFP register space (from 8000h to FFFFh) is logically divided into 8 pages with each page starting at even hex thousand, that is, 8000h, 9000h, A000h, …, F000h, with each page further divided into 32 tables.
The CFP MSA specifies the starting address of all non-volatile registers (NVR) at 8000h (8 NVR tables in total).
Page A000h is allocated for volatile registers (VR). The CFP MSA specifies four VR tables for module configuration, control, and various DDM related functions.

Start Address (hex)	End Address (hex)	Table Name and Description
0000	7FFF	Reserved for IEEE 802.3 use
8000	807F	CFP NVR 1. Basic ID registers
8080	80FF	CFP NVR 2. Extended ID registers
8100	817F	CFP NVR 3. Network lane specific registers
8180	81FF	CFP NVR 4
8200	83FF	MSA Reserved
8400	847F	Vendor NVR 1. Vendor data registers
8480	84FF	Vendor NVR 2. Vendor data registers
8500	87FF	Reserved by CFP MSA
8800	887F	User NVR 1. User data registers
8880	88FF	User NVR 2. User data registers
8900	8EFF	Reserved by CFP MSA
8F00	8FFF	Reserved for User private use
9000	9FFF	Reserved for vendor private use
A000	A07F	CFP Module VR 1. CFP Module level control and DDM registers
A080	A0FF	MLG VR 1. MLG Management Interface registers
A100	A1FF	Reserved by CFP MSA
A200	A27F	Network Lane VR 1. Network lane specific registers
A280	A2FF	Network Lane VR 2. Network lane specific registers
A300	A37F	Network Lane VR 3. Network Lane n Vendor Specific FAWS Registers
A380	A3FF	Reserved by CFP MSA
A400	A47F	Host Lane VR 1. Host lane specific registers
A480	ABFF	Reserved by CFP MSA
AC00	AFFF	Common Data Block Registers
B000	BFFF	Allocated for OIF MSA-100GLH modules
C000	FFFF	Reserved by CFP MSA

Figure 3. Register of a CFPx

9. Ordering Information

Part Number	Description
CF2QD040C10D	CFP2 ER4, 1310nm LAN-WDM, Tx (EML), Rx (PIN+SOA), maximum distance 40km on SMF, 100GBASE-LR4 & OTN OTU4, dual LC connector, 0°C to 70°C, DDM

10. Document Revision Information

Revision	Description
A	Initial release

Skylane Optics® supplies a broad range of optical transceivers. Our engineers work closely with our customers to find the best solutions for every application. We are committed to provide high quality products and services to our customers.

For questions on this product please contact:
support@skylaneoptics.com