CFPQD040C10D – CFP Dual Fibre

1310nm* / 40km / 100GBASE-ER4 & OTN OTU4

*1310NM LAN-WDM 800GHz

For your product safety, please read the following information carefully before any manipulation of the transceiver:

ESD
This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.

LASER SAFETY
This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

1. Overview

CFPQD040C10D is a high performance CFP transceiver module for 100 Gigabit Ethernet and OTN OTU4 data links over a single mode fibre pair. The maximum reach is 40km. The four transmitters are cooled 1310nm LAN-WDM Electro-Absorption Modulated Lasers (EML) generating four optical 25Gbps output signals, which are multiplexed together at the optical output port. The receiver consists of four PIN photodiodes and a Semiconductor Optical Amplifier (SOA) which detect (after optical de-multiplexing) the four 25Gbps optical input signals.
This transceiver module is compliant with the CFP Multisource Agreement (MSA) and hot pluggable. Always contact Skylane Optics commercial agents for compatibility with different equipment platforms.

2. Features

- CFP Multi-Source Agreement compliant
- Hot pluggable CFP footprint
- Supports 103.125 and 111.810Gbps Data Rates
- CAUI-10 Electrical Interface
- Dual LC Optical Connector
- 4× cooled 1310nm LAN-WDM EML Transmitters
- 4× PIN Receivers + SOA
- Up to 40km Point-to-Point Transmission on Single Mode Fibre
- Operating temperature range 0°C to 70°C
- Power Dissipation <16W
- Single +3.3V Power Supply
- CFP MSA MDIO Management Interface

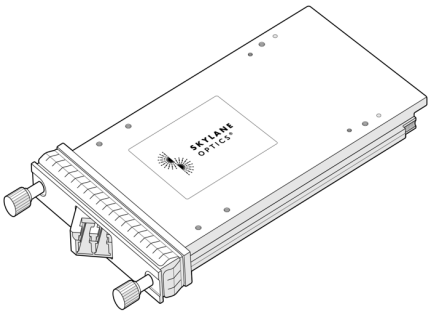

Figure 1. CFP Dual Fibre
(non-binding illustration)

3. Applications

- IEEE 802.3ba 100GBASE-ER4
- ITU-T G.959.1 4I1-9C1F

4. Optical Interface

P/N	Wavelength	Protocol	Optical Output Power[1] [dBm]	Stressed Receiver Sensitivity[2] (OMA) [dBm]	Optical Receiver Overload[3] [dBm]	Link Length[1,4] [km]
CFPQD040C10D	1310nm LAN-WDM 800GHZ	100GBASE-ER4	3.1 to 8.9	≤ -17.9	4.5	≤ 40
		Protocol	**Optical Output Power[1] [dBm]**	**Equivalent Receiver Sensitivity[5] [dBm]**	**Optical Receiver Overload[3] [dBm]**	
		G.959.1 4I1-9C1F	3.1 to 8.9	≤ -23.2	4.5	

1. EOL over operating temperature range
2. 25.78Gbps, BER≤ 10-12, PRBS 231-1, each lane
3. The optical input to each lane of the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used
4. Cabled optical fibre as per IEEE 802.3-2012
5. BER≤10-12, ER≥8dB, with FEC. The BER can be significantly higher at the input to the FEC decoder

5. Technical Parameters

5.1. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit	Notes
Storage temperature	-40		85	°C	
Operating Case Temperature	0		70	°C	
Relative Humidity	5		85	%	Non-Condensing
Power Supply Voltage	3.2	3.3	3.4	V	
Power Supply Current			4850	mA	
Power Dissipation			16	W	

5.2. Transmitter Optical Specifications

100GBASE-ER4					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Data Rate, each Lane		25.78125		Gbps	6
Aggregated Data Rate		103.125		Gbps	6
Average Output Power			8.9	dBm	7
Average Output Power, each Lane	-2.9		2.9	dBm	7,8
Launched OMA, each Lane	0.1		4.5	dBm	7
Difference in launched Power between any two Lanes			3.6	dB	9
Centre Wavelength, Optical Lanes 0 to 3	1294.53	1295.56	1296.59	nm	
	1299.02	1300.05	1301.09		
	1303.54	1304.58	1305.63		
	1308.09	1309.14	1310.19		
Transmitter and Dispersion Penalty (TDP), each Lane			2.5	dB	
Extinction Ratio, each Lane	8			dB	
4I1-9C1F					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Data Rate, each Lane		27.952		Gbps	10
Aggregated Data Rate		111.810		Gbps	10
Average Output Power			8.9	dBm	7
Average Output Power, each Lane	-2.7		2.9	dBm	7
Output Power Difference between any two Lanes			3.6	dB	
Centre Wavelength, Optical Lanes 0 to 3	1294.53	1295.56	1296.59	nm	
	1299.02	1300.05	1301.09		
	1303.54	1304.58	1305.63		
	1308.09	1309.14	1310.19		
Optical Path Penalty			2.5	dB	
Extinction Ratio, each Lane	8			dB	

6. IEEE 802.3ba-2012
7. Output power coupled into a 9/125 µm single mode fibre
8. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
9. Average and OMA
10. ITU-T G.959.1 (02/12), optical interface 4I1-9C1F

5.3. Receiver Optical Specifications					
100GBASE-ER4					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Operating Wavelength, Optical Lanes 0 to 3	1294.53	1295.56	1296.59	nm	
	1299.02	1300.05	1301.09		
	1303.54	1304.58	1305.63		
	1308.09	1309.14	1310.19		
Average Receive Power, each Lane	-20.9		4.5	dBm	11
Receiver Sensitivity (OMA), each Lane			-21.4	dBm	12
Stressed Receiver Sensitivity (OMA), each Lane			-17.9	dBm	13
Difference in receive power between any two lanes (OMA)			4.5	dB	9
4I1-9C1F					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Notes**
Operating Wavelength, Optical Lanes 0 to 3	1294.53	1295.56	1296.59	nm	
	1299.02	1300.05	1301.09		
	1303.54	1304.58	1305.63		
	1308.09	1309.14	1310.19		
Average Receive Power, each Lane	-20.7		4.5	dBm	14
Equivalent Receiver Sensitivity, each Lane			-23.2	dBm	14
Input Power Difference between any two Lanes			4.5	dB	

11. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
12. Receiver sensitivity (OMA), each lane (max) is informative
13. 25.78Gbps, BER≤10-12, PRBS 231-1
14. 27.95Gbps, BER≤10-12, ER≥8dB, with FEC. The BER can be significantly higher at the input to the FEC decode

6. Transceiver Electrical Pad Layout

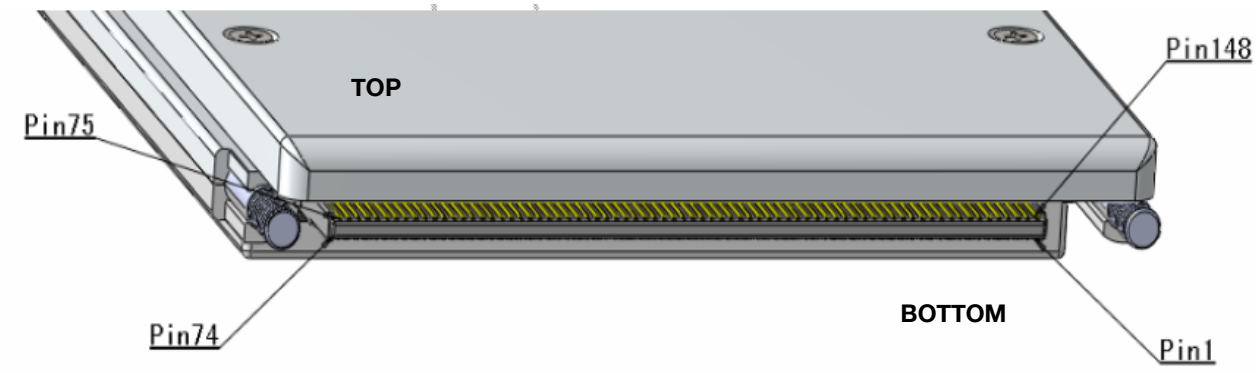

Figure 2. Transceiver Electrical Pad Layout

7. Module Pin Assignment

Pin	Symbol	I/O	Description	Logic	Pin	Symbol	I/O	Description	Logic
1	GND		Ground		75	GND		Ground	
2	GND				76	RX_MCLKp	O	Not for normal use	
3	GND				77	RX_MCLKn			
4	GND				78	GND		Ground	
5	GND				79	RX0p	O	CAUI ch0 Receive Output	CML

6	3.3V		3.3V Power Supply		80	RX0n			
7	3.3V				81	GND		Ground	
8	3.3V				82	RX1p	O	CAUI ch1 Receive Output	CML
9	3.3V				83	RX1n			
10	3.3V				84	GND		Ground	
11	3.3V				85	RX2p	O	CAUI ch2 Receive Output	CML
12	3.3V				86	RX2n			
13	3.3V				87	GND		Ground	
14	3.3V				88	RX3p	O	CAUI ch3 Receive Output	CML
15	3.3V				89	RX3n			
16	GND		Ground		90	GND		Ground	
17	GND				91	RX4p	O	CAUI ch4 Receive Output	CML
18	GND				92	RX4n			
19	GND				93	GND		Ground	
20	GND				94	RX5p	O	CAUI ch5 Receive Output	CML
21	VND_IO_A	I/O	Do not connect		95	RX5n			
22	VND_IO_B				96	GND		Ground	
23	GND		Ground		97	RX6p	O	CAUI ch6 Receive Output	CML
24	TX_MCLKn	O	Not for normal use		98	RX6n			
25	TX_MCLKp				99	GND		Ground	
26	GND		Ground		100	RX7p	O	CAUI ch7 Receive Output	CML
27	VND_IO_C	I/O	Do not connect		101	RX7n			
28	VND_IO_D				102	GND		Ground	
29	VND_IO_E				103	RX8p	O	CAUI ch8 Receive Output	CML
30	PRG_CNTL1	I	Programmable Control 1	LVCMOS w/ PUR	104	RX8n			
31	PRG_CNTL2		Programmable Control 2		105	GND		Ground	
32	PRG_CNTL3		Programmable Control 3		106	RX9p	O	CAUI ch9 Receive Output	CML
33	PRG_ALRM1	O	Programmable Alarm 1	LVCMOS	107	RX9n			
34	PRG_ALRM2		Programmable Alarm 2		108	GND		Ground	
35	PRG_ALRM3		Programmable Alarm 3		109	NC		Do not connect	
36	TX_DIS	I	Transmitter Disable	LVCMOS w/ PUR	110	NC			
37	MOD_LOPWR	I	Module Low Power Mode		111	GND		Ground	
38	MOD_ABS	O	Module Absent Indicator	GND	112	GND			
39	MOD_RSTn	I	Module Reset	LVCMOS w/ PDR	113	TX0p	I	CAUI ch0 Transmit Input	CML
40	RX_LOS	O	Loss of Optical Input Signal	LVCMOS	114	TX0n			
41	GLB_ALRMn	O	Global Alarm	LVCMOS (open drain)	115	GND		Ground	
42	PRTADR4	I	MDIO Physical Port addr. bit4	1.2V CMOS	116	TX1p	I	CAUI ch1 Transmit Input	CML
43	PRTADR3		MDIO Physical Port addr. bit3		117	TX1n			
44	PRTADR2		MDIO Physical Port addr. bit2		118	GND		Ground	
45	PRTADR1		MDIO Physical Port addr. bit1		119	TX2p	I	CAUI ch2 Transmit Input	CML
46	PRTADR0		MDIO Physical Port addr. bit0		120	TX2n			
47	MDIO	I/O	Management bi-dir. Data	1.2V CMOS	121	GND		Ground	

48	MDC	I	Management Data Clock	1.2V CMOS	122	TX3p	I	CAUI ch3 Transmit Input	CML
49	GND		Ground		123	TX3n			
50	VND_IO_F	I/O	Do not connect		124	GND		Ground	
51	VND_IO_G				125	TX4p	I	CAUI ch4 Transmit Input	CML
52	GND		Ground		126	TX4n			
53	VND_IO_H	I/O	Do not connect		127	GND		Ground	
54	VND_IO_J				128	TX5p	I	CAUI ch5 Transmit Input	CML
55	GND		Ground		129	TX5n			
56	GND				130	GND		Ground	
57	GND				131	TX6p	I	CAUI ch6 Transmit Input	CML
58	GND				132	TX6n			
59	GND				133	GND		Ground	
60	3.3V		3.3V Power Supply		134	TX7p	I	CAUI ch7 Transmit Input	CML
61	3.3V				135	TX7n			
62	3.3V				136	GND		Ground	
63	3.3V				137	TX8p	I	CAUI ch8 Transmit Input	CML
64	3.3V				138	TX8n			
65	3.3V				139	GND		Ground	
66	3.3V				140	TX9p	I	CAUI ch9 Transmit Input	CML
67	3.3V				141	TX9n			
68	3.3V				142	GND		Ground	
69	3.3V				143	NC		Do not connected	
70	GND		Ground		144	NC			
71	GND				145	GND		Ground	
72	GND				146	REFCLKp	I	Reference Clock Input	CML
73	GND				147	REFCLKn			
74	GND				148	GND		Ground	

8. Register Allocation

The total CFP register space (from 8000h to FFFFh) is logically divided into 8 pages with each page starting at even hex thousand, that is, 8000h, 9000h, A000h, …, F000h, with each page further divided into 32 tables.
The CFP MSA specifies the starting address of all non-volatile registers (NVR) at 8000h (8 NVR tables in total).
Page A000h is allocated for volatile registers (VR). The CFP MSA specifies four VR tables for module configuration, control, and various DDM related functions.

Start Address (hex)	End Address (hex)	Table Name and Description
0000	7FFF	Reserved for IEEE 802.3 use
8000	807F	CFP NVR 1. Basic ID registers
8080	80FF	CFP NVR 2. Extended ID registers
8100	817F	CFP NVR 3. Network lane specific registers
8180	81FF	CFP NVR 4
8200	83FF	MSA Reserved
8400	847F	NVR 1, Vendor data registers
8480	84FF	NVR 2, Vendor data registers
8500	87FF	Reserved by CFP MSA
8800	887F	NVR 1, User data registers
8880	88FF	NVR 2, User data registers
8900	8EFF	Reserved by CFP MSA
8F00	8FFF	Reserved for User private use
9000	9FFF	Reserved for vendor private use
A000	A07F	CFP Module VR 1. CFP Module level control and DDM registers
A080	A0FF	MLG VR 1. MLG Management Interface registers
A100	A1FF	Reserved by CFP MSA
A200	A27F	Network Lane VR 1. Network lane specific registers
A280	A2FF	Network Lane VR 2. Network lane specific registers
A300	A37F	Network Lane VR 3. Network Lane and Vendor Specific FAWS Registers
A380	A3FF	Reserved by CFP MSA
A400	A47F	Host Lane VR 1. Host lane specific registers
A480	ABFF	Reserved by CFP MSA
AC00	AFFF	Common Data Block Registers
B000	BFFF	Allocated for OIF MSA-100GLH modules
C000	FFFF	Reserved by CFP MSA

Figure 3. Register of a CFP

9. Ordering Information

Part Number	Description
CFPQD040C10D	CFP ER4, 1310nm LAN-WDM, Tx (EML), Rx (PIN+SOA), maximum distance 40km on SMF, 100GBASE-LR4 & OTN OTU4, dual LC connector, 0°C to 70°C, DDM

10. Document Revision Information

Revision	Description
A	Initial release

Skylane Optics supplies a broad range of optical transceivers. Our engineers work closely with our customers to find the best solutions for every application. We are committed to provide high quality products and services to our customers.

For questions on this product please contact:
support@skylaneoptics.com