

QBPQL010E00F – QSFP-DD Dual Fibre / PAM4

ITU CWDM / 10km / 400 Gigabit Ethernet LR4

For your product safety, please read the following information carefully before any manipulation of the transceiver:



ESD

This transceiver is specified as ESD threshold 1kV for SFI pins and 2kV for all others electrical input pins, tested per MIL-STD-883G, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module.



LASER SAFETY

This is a Class1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

The optical ports of the module need to be terminated with an optical connector or with a dust plug in order to avoid contamination.

1. Overview

QBPQL010E00F is a high performance QSFP-DD transceiver module for 400 Gigabit Ethernet data links over a single mode fibre pair. The maximum reach is 10km. An internal gearbox converts the 8 electrical input channels (each 25GBd PAM4) into four 50GBd PAM4 signals. The four transmitters are CWDM lasers generating four optical 50GBd output signals, which are multiplexed together at the optical output port.

The four receivers are PIN photodiodes which detect (after optical de-multiplexing) four 50GBd PAM4 optical input signals. These 50GBd data streams are converted into eight 25GBd electrical output signals by the gearbox.

This transceiver module is compliant with the QSFP-DD Multisource Agreement (MSA) and hot pluggable. Always contact Skylane Optics® commercial agents for compatibility with different equipment platforms.

2. Features

- QSFP-DD Multi-Source Agreement compliant
- Hot pluggable QSFP-DD footprint
- Supports 425Gbps Data Rate
- 8× 26.5625GBd PAM4 Serial Electrical Interface (400GAUI-8)
- 100G Lambda MSA compliant
- Dual LC Optical Interface
- 4× CWDM Transmitters
- 4× PIN Receivers
- Built-in Gearbox / dual CDR
- Up to 10km Point-to-Point Transmission on Single Mode Fibre
- Operating temperature range 0°C to 70°C
- Power Dissipation < 13W
- Single +3.3V Power Supply

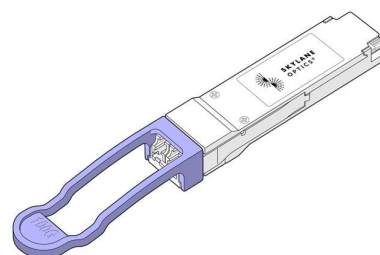


Figure 1. QSFP-DD LC
(non-binding illustration)

3. Applications

- 400Gigabit Ethernet interconnect

4. Optical Interface

P/N	Wavelength	Protocol	Optical Output Power ¹ [dBm]	Stressed Receiver Sensitivity ² (OMA) [dBm]	Optical Receiver Overload ³ [dBm]	Link Length ^{1,4} [km]
QBPQL010E00F	ITU CWDM	400GBASE	3.2 to 10.0	≤ -4.1	4.0	≤ 10

1. EOL over operating temperature range

2. 53.125GBd, BER≤2.4×10⁻⁴, PRBS31Q, pre-FEC, each lane

3. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used

4. Cabled optical fibre as per 100G-FR and 100G-LR Technical Specifications Rev 2.0

5. Technical Parameters

5.1. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit	Notes
Storage temperature	-40		85	°C	
Operating Case Temperature	0		70	°C	
Relative Humidity			85	%	Non-Condensing
Power Supply Voltage	3.135	3.3	3.465	V	
Power Supply Current			4.15	A	
Power Dissipation			13	W	

5.2. Transmitter Optical Specifications

Parameter	Min	Typ	Max	Unit	Notes
Signalling Rate, each Lane		53.125		GBd	5
Aggregated Data Rate		425		Gbps	5
Total Average Output Power	3.2		10.0	dBm	6
Average Output Power, each Lane	-2.8		4.0	dBm	6, 7
Launched Outer OMA (OMA _{outer}), each Lane	0.2		4.2	dBm	6, 8
Difference in Launch Power between any two Lanes (OMA _{outer})			4	dB	
Launched Outer OMA minus TDECQ, each Lane	-1.2			dBm	6, 9
	-1.1				6, 10
Centre Wavelength, Optical Lanes 0 to 3	1264.5	1271	1277.5	nm	
	1284.5	1291	1297.5		
	1304.5	1311	1317.5		
	1324.5	1331	1337.5		
Transmitter and Dispersion Eye Closure (TDECQ), each Lane			3.9	dB	
Extinction Ratio, each Lane	3.5			dB	

5. IEEE 802.3bs-2017

6. Output power coupled into a 9/125 µm single mode fibre

7. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance

8. Even if the TDECQ < 1.2dB for an extinction ratio of ≥ 4.5dB or TDECQ < 1.1dB for an extinction ratio of < 4.5dB, the minimum OMA_{outer} must exceed 0.2dBm

9. Extinction ratio ≥ 4.5dB

10. Extinction ratio < 4.5dB

5.3. Receiver Optical Specifications

Parameter	Min	Typ	Max	Unit	Notes
Operating Wavelength, Optical Lanes 0 to 3	1264.5	1271	1277.5	nm	
	1284.5	1291	1297.5		
	1304.5	1311	1317.5		
	1324.5	1331	1337.5		
Average Receive Power, each Lane	-9.1		4.0	dBm	11
Receive Power (OMA _{outer}), each Lane			4.2		
Difference in Receive Power between any two Lanes (OMA _{outer})			4.1	dB	
Receiver Sensitivity (OMA _{outer}), each Lane			-4.1	dBm	12
Stressed Receiver Sensitivity (OMA _{outer}), each Lane			-4.1	dBm	13

11. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance

12. Receiver sensitivity (OMA), each lane (max) is informative and is defined for a transmitter with SECQ of 3.9 dB

13. 53.125GBd, BER≤2.4×10⁻⁴, PRBS31Q, pre-FEC, each lane

6. Transceiver Electrical Pad Layout


















































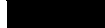
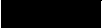
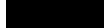
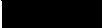




















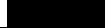
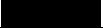
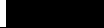
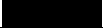
Top side						Bottom side						
38	GND		76	GND				GND	39		GND	1
37	TX1n		75	TX5n				TX6n	40		TX2n	2
36	TX1p		74	TX5p				TX6p	41		TX2p	3
35	GND		73	GND				GND	42		GND	4
34	TX3n		72	TX7n				TX8n	43		TX4n	5
33	TX3p		71	TX7p				TX8p	44		TX4p	6
32	GND		70	GND				GND	45		GND	7
31	LPMODE		69	Reserved				Reserved	46		ModSelL	8
30	Vcc1		68	Vcc2				VS1	47		ResetL	9
29	VccTx		67	VccTx1				VccRx1	48		VccRx	10
28	IntL		66	Reserved				VS2	49		SCL	11
27	ModPrsL		65	NC				VS3	50		SDA	12
26	GND		64	GND				GND	51		GND	13
25	RX4p		63	RX8p				RX7p	52		RX3p	14
24	RX4n		62	RX8n				RX7n	53		RX3n	15
23	GND		61	GND				GND	54		GND	16
22	RX2p		60	RX6p				RX5p	55		RX1p	17
21	RX2n		59	RX6n				RX5n	56		RX1n	18
20	GND		58	GND				GND	57		GND	19
Legacy QSFP28 pads			Additional QSFP-DD pads				Additional QSFP-DD pads			Legacy QSFP28 pads		

Figure 2. QSFP-DD Electrical Pad Layout

7. Module Electrical Pin Definition

Pin Number	Name	Function	Pin Number	Name	Function
1	GND	Ground	39	GND	Ground
2	TX2n	Transmitter Inverted Data Input	40	TX6n	Transmitter Inverted Data Input
3	TX2p	Transmitter Non-Inverted Data Input	41	TX6p	Transmitter Non-Inverted Data Input
4	GND	Ground	42	GND	Ground
5	TX4n	Transmitter Inverted Data Input	43	TX8n	Transmitter Inverted Data Input
6	TX4p	Transmitter Non-Inverted Data Input	44	TX8p	Transmitter Non-Inverted Data Input
7	GND	Ground	45	GND	Ground
8	ModSelL	Module Select	46	Reserved	For future use
9	ResetL	Module Reset	47	VS1	Module Vendor Specific 1
10	VccRx	+3.3V Power Supply Receiver	48	VccRx1	3.3V Power Supply
11	SCL	2-wire serial interface clock	49	VS2	Module Vendor Specific 2
12	SDA	2-wire serial interface data	50	VS3	Module Vendor Specific 3
13	GND	Ground	51	GND	Ground
14	RX3p	Receiver Non-Inverted Data Output	52	RX7p	Receiver Non-Inverted Data Output
15	RX3n	Receiver Inverted Data Output	53	RX7n	Receiver Inverted Data Output
16	GND	Ground	54	GND	Ground
17	RX1p	Receiver Non-Inverted Data Output	55	RX5p	Receiver Non-Inverted Data Output
18	RX1n	Receiver Inverted Data Output	56	RX5n	Receiver Inverted Data Output
19	GND	Ground	57	GND	Ground
20	GND	Ground	58	GND	Ground
21	RX2n	Receiver Inverted Data Output	59	RX6n	Receiver Inverted Data Output
22	RX2p	Receiver Non-Inverted Data Output	60	RX6p	Receiver Non-Inverted Data Output
23	GND	Ground	61	GND	Ground
24	RX4n	Receiver Inverted Data Output	62	RX8n	Receiver Inverted Data Output
25	RX4p	Receiver Non-Inverted Data Output	63	RX8p	Receiver Non-Inverted Data Output
26	GND	Ground	64	GND	Ground
27	ModPrsL	Module Present	65	NC	No Connect
28	IntL	Interrupt	66	Reserved	For future use
29	VccTx	+3.3V Power supply transmitter	67	VccTx1	3.3V Power Supply
30	Vcc1	+3.3V Power supply	68	Vcc2	3.3V Power Supply
31	LPMODE	Low Power Mode	69	Reserved	For future use
32	GND	Ground	70	GND	Ground
33	TX3p	Transmitter Non-Inverted Data Input	71	TX7p	Transmitter Non-Inverted Data Input
34	TX3n	Transmitter Inverted Data Input	72	TX7n	Transmitter Inverted Data Input
35	GND	Ground	73	GND	Ground
36	TX1p	Transmitter Non-Inverted Data Input	74	TX5p	Transmitter Non-Inverted Data Input
37	TX1n	Transmitter Inverted Data Input	75	TX5n	Transmitter Inverted Data Input
38	GND	Ground	76	GND	Ground

The diagram illustrates the memory map of the device, organized into three main sections: Lower Page (00h-7Fh), Main Memory (80h-FFh), and Bank Page (10h-1Fh).

Lower Page (00h-7Fh):

- 00h: Module Dynamic Information (VRs)
- 7Eh: Bank Select
- 7Fh: Page Select

Main Memory (80h-FFh):

- Page 00h: System ID, Advertising (NVRs)
- Page 01h: Revision codes Advertising (NVRs)
- Page 02h: Module and Lane Threshold Values (NVRs)
- Page 03h: User EEPROM (NVRs)
- Page 04h: Tunable Laser Advertising (NVRs)
- Pages 05h-0Fh: Reserved
- Pages B0h-FFh: Custom

Bank Page (10h-1Fh):

- 10h: Bank Control
- 11h: Bank Flags
- 12h: WDM
- 13h-14h: Diagnostic
- 15-1Dh: Reserved
- 1E-1Fh: Custom

Bank Mapping:

- Bank N Pages (10h-1Fh):** Bank N Pages 10h-1Fh, Bank 1 Pages 10h-1Fh, Bank 0 Pages 10h-1Fh. Lane Dynamic Information (VRs).
- Bank N Pages (20h-3Fh):** Bank N Pages 20h-3Fh, Bank 1 Pages 20h-3Fh, Bank 0 Pages 20h-3Fh. Reserved For Coherent.
- Pages 40h-4Fh:** Reserved For Coherent.
- Pages 50h-9Eh:** Reserved.
- Bank 1 Page 9Fh:** Command and local Payload For CDB.
- Bank 0 Page 9Fh:** Extended Payload For CDB.

Bank Dependent Pages:

- Bank N Pages 10h-1Fh
- Bank 1 Pages 10h-1Fh
- Bank 0 Pages 10h-1Fh
- Bank N Pages 20h-3Fh
- Bank 1 Pages 20h-3Fh
- Bank 0 Pages 20h-3Fh
- Bank 1 Page 9Fh
- Bank 0 Page 9Fh

Banks > 0 Reserved:

- Pages 40h-4Fh
- Pages 50h-9Eh

Bank Dependent Pages:

- Bank 1 Pages A0h-AFh
- Bank 0 Pages A0h-AFh

9. Ordering Information

Part Number	Description
QBPQL010E00F	QSFP-DD LR4, PAM4, CWDM, Tx (EML), Rx (PIN), maximum distance 10km on SMF, 400 Gigabit Ethernet, dual LC, Pull-Tab, 0°C to 70°C, DDM

10. Document Revision Information

Revision	Description
A	Initial release

Skylane Optics® supplies a broad range of optical transceivers. Our engineers work closely with our customers to find the best solutions for every application. We are committed to provide high quality products and services to our customers.

For questions on this product please contact:

support@skylaneoptics.com

**Beyond
Quality**

**Reliable
Alliance**

**Performing
Smartly**